CLAIMS

What is claimed is:

1. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip; and

a multimedia processor block incorporated on the IC chip.

2. Multimedia interface, according to claim 1, wherein:

the reconfigurable logic is a field programmable gate array (FPGA).

3. Multimedia interface, according to claim 1, further comprising at least one functional block selected from the group consisting of:

audio and/or video CODECs for interfacing to external analog multimedia signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

power-down circuitry, in combination with one or more of these additional cores.

4. Multimedia interface, according to claim 1, wherein:

the processor block is implemented with 20k-40k gates; and

the reconfigurable logic block is implemented with at least 60k gates, including at least 80k gates, including at least 100k gates.

5. Multimedia interface, according to claim 1, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with approximately 10k gates.

6. Multimedia interface, according to claim 1, wherein:

the processor block is implemented with a first number (P) of gates; and

the reconfigurable logic block is implemented with a second number (L) of gates;

wherein:

the second number (L) is at least three times greater than the first number (P).

7. Multimedia interface, according to claim 6, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the second number (L) is at least six times greater than the third number (C).

8. Multimedia interface, according to claim 6, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the first number (P) is 2-4 times greater than the third number (C).

9. Multimedia interface, according to claim 1, wherein:

the processor block is implemented with a first number (P) of gates; and

the reconfigurable logic block is implemented with a second number (L) of gates;

wherein:

the second number (L) is at least four times greater than the first number (P).

10. Multimedia interface, according to claim 9, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the second number (L) is at least six times greater than the third number (C).

11. Multimedia interface, according to claim 9, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the first number (P) is 2-4 times greater than the third number (C).

12. Multimedia interface, according to claim 1, wherein:

the processor block is implemented with a first number (P) of gates; and

the reconfigurable logic block is implemented with a second number (L) of gates;

wherein:

the second number (L) is at least five times greater than the first number (P).

13. Multimedia interface, according to claim 12, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the second number (L) is at least six times greater than the third number (C).

14. Multimedia interface, according to claim 12, further comprising:

a CODEC block incorporated on the IC chip;

wherein:

the CODEC block is implemented with a third number (C) of gates; and

the first number (P) is 2-4 times greater than the third number (C).

15. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip; and

a RISC core incorporated on the IC chip.

16. Signal processing interface, according to claim 15, wherein:

the reconfigurable logic is a field programmable gate array (FPGA).

17. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip; and

a CODEC incorporated on the IC chip.

18. Signal processing interface, according to claim 17, wherein:

the reconfigurable logic is a field programmable gate array (FPGA).

19. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip; and

a serial link incorporated on the IC chip.

20. Signal processing interface, according to claim 19, wherein:

the reconfigurable logic is a field programmable gate array (FPGA).

21. An electronic system incorporating at least one integrated circuit (IC chip), said IC chip comprising:

a block of reconfigurable logic incorporated on the IC chip; and

a multimedia processor block incorporated on the IC chip.

22. An electronic system, according to claim 21, wherein the electronic system is selected from the group consisting of general-purpose computer, telecommunication device, network device, consumer device, receiver, recorder, display device, and vehicle.